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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/213,271	12/17/1998	MARTIN R. HANDFORTH	RO-3951	7176

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EXAMINER
TRAN, CON P

ART UNIT	PAPER NUMBER
2644	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/213,271	HANDFORTH ET AL.	
	Examiner	Art Unit	
	Con P. Tran	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *10* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1 recites the limitation "the isolation means" in line 6. The claim is rejected as failing to provide proper antecedent basis for this limitation in the claim. It is unclear whether "the isolation means" refers to "isolation means" or "line circuit isolation means". Examiner assumes it is referred to the "isolation means" in line 5. This Office Action is based on that assumption.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1, 7-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hung et al. U.S. Patent 5,390,231 in view of Pistilli U.S. Patent 5,539,820 (cited by Applicant).

Regarding claim 1, Hung et al. teaches a protection arrangement for a line circuit (see Fig. 1, and respective portions of the specification), comprising:

current sensing means (12) for sensing current flowing through the telephone subscriber line (see col. 5, lines 20-30);

line circuit isolation means (contacts 14, relay 15) for selectively coupling the line circuit to the telephone subscriber line (see col. 5, lines 20-30);

However, Hung et al. does not explicitly show:

isolation means for selectively coupling a power supply to the line circuit; and control means for operating the isolation means to decouple the power supply from the line circuit in response to a current sensed, by the current sensing means exceeding a current threshold, and to recouple the power supply to the line circuit responsive to a predetermined time interval having passed.

Hung et al. teaches the digital control circuit 20 controls the voltage DV and the voltages TV and RV to provide a limited loop current while maintaining adequate voltage via amplifier 32 (col. 6, lines 40-50).

Thus one of ordinary skill would have been motivated to seek interface circuit having an isolation means for selectively coupling a power supply to the line circuit; and control means for operating the isolation means embodiment in order to isolate and control of an actual working arrangement taught by Hung et al.. Such embodiments would have been any known isolation means and control means such as one of Pistilli in the same field of endeavor.

Pistilli teaches (Fig. 1) a CVG 20, a switch S which is closed so that the battery voltage BV is connected to the line 22 to constitute the line drive circuit supply voltage DV (see col. 5, lines 17-22). In addition, Pistilli further teaches the line interface circuit illustrated in FIG. 4 includes diode 54, transistor 48. The transistor 48 is fully turned on, its collector current flowing through the resistor 46 reducing the gate-source voltage of the MOSFET 42 to turn off this MOSFET, so that current is no longer supplied via the line 22 to the capacitor 26 (col. 9, lines 17-42) in order to substantially eliminate current through the controlled path of the transistor (col. 3, lines 34-36).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to include within the Hung et al. a interface circuit as taught by Pistilli in order to substantially eliminate current through the controlled path of the transistor as suggested by Pistilli in column 3, lines 34-36.

Regarding **claim 7**, Hung et al. teaches a method of protecting a line circuit connected to a power supply (CVG 18; col. 5, lines 32-42) and to a telephone subscriber line from an over-current condition (see Fig. 1, 2, and respective portions of the specification), the over-current condition being defined as when current flowing through the telephone subscriber line exceeds a predetermined current threshold value (see col. 7, lines 40-47), comprising the steps of:

a) checking for a presence of the over-current condition (see col. 7 lines 48-50);

b) starting, responsive to the over-current condition being present, a timer of predetermined duration (see col. 7 lines 56-59);

c) disconnecting, responsive to the timer having expired, the line circuit (see col. 8 lines 42-46);

d) waiting a predetermined amount of time (see col. 9 lines 7-12); and

e) reconnecting the line circuit (see col. 7 lines 18-25).

However, Hung et al. does not explicitly show:

steps of power supply being disconnected, reconnected from line circuit.

Hung et al. teaches the digital control circuit 20 controls the voltage DV and the voltages TV and RV to provide a limited loop current while maintaining adequate voltage via amplifier 32 (col. 6, lines 40-50).

Thus one of ordinary skill would have been motivated to seek a method in which an interface circuit protection having steps of power supply being disconnected, reconnected from line circuit in order to provide a method for an actual working arrangement taught by Hung et al.. Such embodiments would have been any known method of protection interface circuit such as one of Pistilli in the same field of endeavor.

Pistilli teaches (Fig. 1) a CVG 20, a switch S which is closed so that the battery voltage BV (i.e. a separate power supply) is connected to the line 22 to constitute the line drive circuit supply voltage DV (see col. 5, lines 17-22). In addition, Pistilli further teaches the line interface circuit illustrated in FIG. 4 includes diode 54, transistor 48. The transistor 48 is fully turned on, its collector current flowing through the resistor 46

reducing the gate-source voltage of the MOSFET 42 to turn off this MOSFET, so that current is no longer supplied via the line 22 to the capacitor 26 (col. 9, lines 17-42) in order to substantially eliminate current through the controlled path of the transistor (col. 3, lines 34-36).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to include within the Hung et al. a method of protection interface circuit as taught by Pistilli in order to substantially eliminate current through the controlled path of the transistor as suggested by Pistilli in column 3, lines 34-36.

Regarding **claim 8**, Hung et al. further teaches a method, wherein the step (b) of starting further comprises the steps of (see Fig. 2, and respective portions of the specification):

checking (block 52), after starting the timer, for the presence of the over-current condition (see col. 7, lines 55-67); and

stopping (block 55), responsive to the over-current condition no longer being present, the timer and continuing the method from the step (a) of checking (see col. 7, line 67 – col. 8, line 6);

Regarding **claim 9**, Hung et al. further teaches a method, wherein the step (b) of starting further comprises the steps of (see Fig. 2, 4 and respective portions of the specification):

checking (block 82), responsive to starting the timer and to the over current condition being present, for a presence of an over-voltage condition (see col. 13,

lines 11-28), the over-voltage condition being defined as when voltage on the telephone subscriber line exceeds a predetermined voltage threshold value (see col. 7, lines 11-20); and

stopping (block 50), responsive to the over-voltage condition being present, the timer and continuing the method from the step (a) of checking (see col. 8, line 7-41).

Regarding **claim 10**, Hung et al. further teaches a method, as claimed in claim 9, wherein the step (b) of starting a timer further comprises the steps of (see Fig. 2, and respective portions of the specification):

checking (block 59), responsive to the over-current condition being present and an over-voltage condition not being present, the timer to determine if the timer has expired (see col. 7, line 55 – col. 8, lines 6); and

continuing (block 51), responsive to the timer not having expired, the method from the step of checking, after starting the timer, for the presence of the over-current condition (see col. 8, lines 7-21).

Regarding **claim 11**, Hung et al. teaches a method of protecting a line circuit (see Fig. 2, 3 and respective portions of the specification) connected to a telephone subscriber line and to a separate power supply (CVG 18; col. 5, lines 32-42) from an over-voltage condition, the over voltage condition being defined as when voltage on the

telephone subscriber line exceeds a predetermined voltage threshold value (see col. 7, lines 11-20), comprising the steps of:

a) checking (block 55) for a presence of the over-voltage condition;

b) starting (block 58), responsive to the over-voltage condition being present, a first timer of predetermined duration;

c) disconnecting (block 61), responsive to the timer having expired and to the over-voltage condition being present, the line circuit from the telephone subscriber line;

d) waiting a predetermined amount of time (see col. 10, lines 52-59); and

e) reconnecting the line circuit to the telephone subscriber line (see col. 10, lines 59-65).

However, Hung et al. does not explicitly show:

steps of power supply being disconnected, reconnected from line circuit and from telephone subscriber line circuit.

Hung et al. teaches the digital control circuit 20 controls the voltage DV and the voltages TV and RV to provide a limited loop current while maintaining adequate voltage via amplifier 32 (col. 6, lines 40-50).

Thus one of ordinary skill would have been motivated to seek a method in which an interface circuit protection having steps of power supply being disconnected, reconnected from line circuit and from telephone subscriber line circuit in order to provide a method for an actual working arrangement taught by Hung et al.. Such

embodiments would have been any known method of protection interface circuit such as one of Pistilli in the same field of endeavor.

Pistilli teaches (Fig. 1) a CVG 20, a switch S which is closed so that the battery voltage BV (i.e. a separate power supply) is connected to the line 22 to constitute the line drive circuit supply voltage DV (see col. 5, lines 17-22). In addition, Pistilli further teaches the line interface circuit illustrated in FIG. 4 includes diode 54, transistor 48. The transistor 48 is fully turned on, its collector current flowing through the resistor 46 reducing the gate-source voltage of the MOSFET 42 to turn off this MOSFET, so that current is no longer supplied via the line 22 to the capacitor 26 (col. 9, lines 17-42) in order to substantially eliminate current through the controlled path of the transistor (col. 3, lines 34-36).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to include within the Hung et al. a method of protection interface circuit as taught by Pistilli in order to substantially eliminate current through the controlled path of the transistor as suggested by Pistilli in column 3, lines 34-36.

Regarding **claim 12**, Hung et al. teaches a method circuit (see Fig. 1, 2 and respective portions of the specification), wherein the method further comprises the steps of:

f) checking (block 55) for the presence of the over-voltage condition;

g) restarting (block 58), responsive to the over-voltage condition being present, the first timer; and

h) disconnecting (block 61), responsive to the first timer having expired after being restarted and to the over-voltage condition being present, the line circuit from the telephone subscriber line (see col. 9, lines 13-30).

Regarding **claim 13**, Hung et al. further teaches a method (see Fig. 1, 2 and respective portions of the specification) as claimed in claim 12, wherein the step (e) of reconnecting further comprises the steps of:

starting a second timer (63) of predetermined duration after the telephone subscriber interface circuit has been reconnected to the telephone subscriber line; and

continuing (block 51), responsive to the second timer having expired and the over-voltage condition not being present, the method from the step (a) of checking (see col. 9, lines 7-12).

Regarding **claim 14**, Hung et al. further teaches a method as claimed in claim 12, wherein the step (b) of starting further comprises the steps of (see Fig. 1, 2 and respective portions of the specification):

checking (block 51), after the first timer has been started, for the presence of the over-voltage condition; and

continuing (block 52), responsive to the over-voltage condition not being present and the first timer not having expired, the method from the step (a) of checking (see col. 9, lines 7-12).

Regarding **claim 15**, Hung et al. further teaches a method as claimed in claim 13, wherein the step (g) of restarting further comprises the steps of (see Fig. 1, 2 and respective portions of the specification):

checking (block 54), after the first timer (block 58) has been restarted, for the presence of the over-voltage condition; and

continuing (block 52), responsive to the over-voltage condition not being present, the method from the step of starting a second timer (see col. 9, lines 7-12).

Regarding **claim 16**, Hung et al. teaches a method (see Fig. 1, 2, 3, 5 and respective portions of the specification) of protecting a line circuit connected to a telephone subscriber line and to a separate power supply (CVG 18; col. 5, lines 32-42) from positive and negative over-voltage conditions (see col. 14, lines 24-33), the positive over-voltage condition being defined as when voltage on the telephone subscriber line exceeds a predetermined positive voltage threshold value and the negative over-voltage condition being defined as when voltage on the telephone subscriber line exceeds a predetermined negative voltage threshold value (see col. 14, lines 40-48), comprising the steps of:

a) checking (block 55) for a presence of the positive over-voltage condition;

b) checking (block 55), responsive to the positive over-voltage condition not being present, for a presence of the negative over-voltage condition;

c) starting (block 58), responsive to the negative over-voltage condition being present, a first timer of predetermined duration;

d) disconnecting (block 61), responsive to the timer having expired and to the negative over-voltage condition being present, the line circuit from the telephone subscriber line;

e) waiting a predetermined amount of time (block 63); and

f) reconnecting (91) the line circuit to the telephone subscriber line (see col. 14, lines 33-39).

However, Hung et al. does not explicitly show:

steps of power supply being disconnected, reconnected from line circuit and from telephone subscriber line circuit.

Hung et al. teaches the digital control circuit 20 controls the voltage DV and the voltages TV and RV to provide a limited loop current while maintaining adequate voltage via amplifier 32 (col. 6, lines 40-50).

Thus one of ordinary skill would have been motivated to seek a method in which an interface circuit protection having steps of power supply being disconnected, reconnected from line circuit and from telephone subscriber line circuit in order to provide a method for an actual working arrangement taught by Hung et al.. Such embodiments would have been any known method of protection interface circuit such as one of Pistilli in the same field of endeavor.

Pistilli teaches (Fig. 1) a CVG 20, a switch S which is closed so that the battery voltage BV (i.e. a separate power supply) is connected to the line 22 to constitute the

line drive circuit supply voltage DV (see col. 5, lines 17-22). In addition, Pistilli further teaches the line interface circuit illustrated in FIG. 4 includes diode 54, transistor 48. The transistor 48 is fully turned on, its collector current flowing through the resistor 46 reducing the gate-source voltage of the MOSFET 42 to turn off this MOSFET, so that current is no longer supplied via the line 22 to the capacitor 26 (col. 9, lines 17-42) in order to substantially eliminate current through the controlled path of the transistor (col. 3, lines 34-36).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to include within the Hung et al. a method of protection interface circuit as taught by Pistilli in order to substantially eliminate current through the controlled path of the transistor as suggested by Pistilli in column 3, lines 34-36.

Regarding claim 17, Hung et al. further teaches a method (see Fig. 1, 2 and respective portions of the specification) a method, wherein the method further comprises the steps of:

g) checking (block 55) for a presence of the positive over-voltage condition;

h) checking (block 55), responsive to the positive over-voltage condition not being present, for a presence of the negative over-voltage condition;

i) restarting (block 58), responsive to the negative over-voltage condition being present, the first timer; and

j) disconnecting (block 61), responsive to the first timer having expired after being restarted and to the negative over-voltage condition being present, the line circuit from the telephone subscriber line.

Regarding **claim 18**, Hung et al. further teaches a method (see Fig. 1, 2, 5 and respective portions of the specification) a method as claimed in claim 17, wherein the step (f) of reconnecting further comprises the steps of:

starting (block 92), after the telephone subscriber interface circuit has been reconnected to the telephone subscriber line, a third timer of predetermined duration;

checking (block 94), for a presence of the positive over-voltage condition;

checking (block 95), responsive to the positive over-voltage condition not being present, for a presence of the negative over-voltage condition; and

continuing (block 55), responsive to the third timer having expired and both positive and negative over-voltage conditions not being present, the method from the step (a) of checking (see col. 15, lines 33-45).

Regarding **claim 19**, Hung et al. further teaches (see Fig. 1, 2, 4 and respective portions of the specification) a method as claimed in claim 17, wherein the step (c) of starting further comprises the steps of:

checking (block 55), after the first timer has been started, for a presence of the positive over-voltage condition;

starting (block 63), responsive to the positive over-voltage condition being present, a second timer of predetermined duration;

disconnecting (block 61), responsive to the second timer having expired and to the positive over-voltage condition being present, the line circuit from the telephone subscriber line;

waiting a predetermined amount of time (block 63); and

reconnecting (block 84) the line circuit to the telephone subscriber line (see col. 13, lines 12-27).

Regarding **claim 20**, Hung et al. further teaches (see Fig. 1, 2 and respective portions of the specification) a method as claimed in claim 18, wherein the step (i) of restarting further comprises the steps of:

checking (block 55), after the first timer (block 58) has been restarted, for a presence of the positive over-voltage condition;

starting (block 63), responsive to the positive over-voltage condition being present, a second timer of predetermined duration; and

disconnecting (block 61711), responsive to the second timer having expired and to the positive over-voltage condition being present, the line circuit from the telephone subscriber line.

Regarding claim 21, Hung et al. further teaches (see Fig. 1, 2 and respective portions of the specification) a method as claimed in claim 20, wherein the step of starting a second timer further comprises the steps of:

checking (block 55), after the second timer has been started, for the presence of the positive over-voltage condition; and

continuing (block 62), responsive to the positive over-voltage condition not being present and the second timer not having expired, the method from the step of starting the third timer.

Regarding claim 22, Hung et al. further teaches (see Fig. 1, 2, 5 and respective portions of the specification) a method as claimed in claim 20, wherein the step of:

checking (block 55) for a presence of the positive over-voltage condition after the first timer has been restarted further comprises the steps of:

checking (block 95), responsive to the positive over-voltage condition not being present, for the presence of the negative over-voltage condition (see col. 15, lines 7-18); and

continuing (block 62), responsive to the negative over-voltage condition not being present and the first timer not having expired after having been restarted, the method from the step of starting the third timer (see col. 14, lines 33-39).

Regarding **claim 23**, Hung et al. further teaches (see Fig. 1, 2, 5 and respective portions of the specification) a method as claimed in claim 16, wherein the step (c) of starting further comprises the steps of:

checking (block 55), after the first timer has been started, for the presence of the negative over-voltage condition; and

continuing (block 51), responsive to the negative over-voltage condition not being present and the first timer not having expired, the method from the step (a) of checking (see col. 7, lines 48-55).

5. **Claims 2-6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hung et al. U.S. Patent 5,390,231 in view of Pistilli U.S. Patent 5,539,820 (cited by Applicant), and further in view of Chen U.S. Patent 6,288,883.

Regarding **claim 2**, Hung et al. in view of Pistilli teaches a protection arrangement for a line circuit a protection arrangement of claim 1. However, Hung et al. and Pistilli in combination does not explicitly disclose an isolation means that comprises:

a FET having a source for connecting to the power supply, a drain for connecting to the line circuit, and a gate; and

an interface circuit connected to the source and drain of the FET, having an input connected to the control means, and an output connected to the gate of the FET, the interface circuit for operating the FET in saturation mode to couple the power

supply to the line circuit and for turning off the FET to decouple the power supply from line circuit.

Thus one of ordinary skill would have been motivated to seek a FET and an interface circuit connected to the source and drain of the FET in order to isolate and control of an actual working arrangement taught by Hung et al. and Pistilli in combination. Such embodiments would have been any known isolation means such as one of Chen in the same field of endeavor.

Chen teaches an isolation means that comprises (see Fig. 2, 3, and respective portions of the specification):

a FET (Q102) having a source (S) for connecting to the power supply (i.e., input 12), a drain (D) for connecting to the line circuit (i.e., output 18), and a gate (G; see col. 3, lines 11-21); and

an interface circuit (see col. 1, lines 20-26) connected to the source (S) and drain (D) of the FET (see col. 3, lines 25-31), having an input connected to the control means (C125), and an output connected to the gate of the FET, the interface circuit for operating the FET in saturation mode to couple the power supply to the line circuit and for turning off the FET to decouple the power supply from line circuit (see col. 4, lines 5-15) in order to provide over-voltage or over-current protection (see col. 2, lines 37-41).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included within the Hung et al. and Pistilli in combination an isolation circuit as taught by Chen since such combination would

provide over-voltage or over-current protection as suggested by Chen in col. 2, lines 37-41.

Regarding **claim 3**, Chen further teaches a protection arrangement (see Fig. 2, 3, and respective portions of the specification), wherein the interface circuit comprises:

a voltage divider having first (R125) and second (126) resistors, the first resistor (125) connected to the source (S) of the FET at one end and to the gate (G) of the FET at the other end, and the second resistor (126) connected to the gate of the FET at one end (see col. 5, lines 25-27); and

a pnp transistor (i.e., Q101, see col. 5, lines 34-38) having a base connected to ground, an emitter coupled to the controller means (C125), and a collector connected to the other end of the second resistor. It should be noted that the Chen reference discloses a npn transistor in drawings (Fig. 3). However, the reference does not explicitly specify a npn transistor in the specification.

Nevertheless, as would have been well known in the art at the time the invention was made, those of ordinary skill in the art would be able to modify the npn transistor in the protection circuit taught by Chen reference with a pnp transistor.

Accordingly, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify the npn transistor in the protection circuit taught by Chen reference with a pnp transistor.

Regarding **claim 4**, Chen further teaches a protection arrangement (see Fig. 2 and 3), wherein the interface circuit further comprises a zener diode (16) having an anode connected to the source of the FET (Q 102) and a cathode connected to the gate of the FET (see col. 3 lines 39-41).

Regarding **claim 5**, Chen further teaches a protection arrangement (see Fig. 3), wherein the interface circuit further comprises a capacitor (C125) connected to the emitter of the pnp transistor at one end and to the drain (D) of the FET (Q102) at the other end (see col. 4 lines 5-11).

Regarding **claim 6**, Chen further teaches a protection arrangement (see Fig. 3), wherein the interface circuit further comprises a resistor (R133) that couples the emitter of the pnp transistor to the controller (C125; see col. 4 lines 16-19).

Response to Arguments

6. Applicant's arguments filed on December 27, 2002 are persuasive. Accordingly, the Hung et al. (4,709,296) is removed.

7. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new grounds of rejection.

Conclusion

8. The following are suggested formats for either a Certificate of Mailing or Certificate of Transmission under 37 CFR 1.8(a). The certification may be included with all correspondence concerning this application or proceeding to establish a date of mailing or transmission under 37 CFR 1.8(a). Proper use of this procedure will result in such communication being considered as timely if the established date is within the required period for reply. The Certificate should be signed by the individual actually depositing or transmitting the correspondence or by an individual who, upon information and belief, expects the correspondence to be mailed or transmitted in the normal course of business by another no later than the date indicated.

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to:

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(Date)

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Please refer to 37 CFR 1.6(d) and 1.8(a)(2) for filing limitations concerning facsimile transmissions and mailing, respectively.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Con P. Tran, whose telephone number is (703) 305-2341. The examiner can normally be reached on M - F (8:30 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forester W. Isen can be reached on (703) 305-4386. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Customer Service Office at telephone number (703) 306-0377.

cpt CPT
March 19, 2003

FORESTER W. ISEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600